

*A1  
concluded* December 2, 1999, which is a divisional of U.S. Patent Application Serial No. 09/119,053, filed July 20, 1998, now U.S. Patent 6,066,881.--.

Page 3, line 10, please delete "23a" and replace it with --23b--.

Page 19, line 9, please delete "9" and replace it with --8--.

Page 24, line 16, please delete "13A and 13B" and replace it with --13--.

IN THE CLAIMS:

Please cancel all claims from the application and replace by the following new claims:

~~--12. A method of manufacturing a semiconductor device, comprising the steps of:~~

~~forming first and second gate electrodes of first and second transistors on a main surface of a semiconductor substrate with a space between each other;~~

~~forming a nitride film covering said first and second gate electrodes;~~

~~forming source/drains of said first and second transistors;~~

~~forming an interlayer insulating film covering said nitride film;~~

~~forming in said interlayer insulating film a first contact hole reaching one of said source/drain of said first transistor;~~

~~providing a second contact hole formed in said interlayer insulating film and reaching one of said source/drain of said second transistor and a third contact hole penetrating said interlayer insulating film and said nitride film reaching said second gate electrode; and~~

~~forming a bit line connected via said first contact hole to one of said source/drain of said~~

*B*  
first transistor, and first and second interconnections extending in said second and third contact holes.

*13.* The method according to claim 12, said source/drain of said second transistor having a highly doped region, wherein:

*Pulse*  
*RECORDED - EPOSSONATE 1/26*  
the step of forming said source/drain of said second transistor includes the step of forming first metal silicide at a surface of said heavily doped region; and

the step of forming said bit line includes the steps of: forming a plug electrode in said first contact hole; forming second metal silicide at a surface of said plug electrode; and forming said bit line on said second metal silicide.

*14.* A method of manufacturing a semiconductor device, comprising the steps of:  
forming first and second gate electrodes of first and second transistors on a main surface of a semiconductor substrate with a space between each other;  
forming a nitride film covering side walls of said first and second gate electrodes;  
forming first impurity regions at opposite sides of said first and second gate electrodes;  
forming an interlayer insulating film covering said first and second gate electrodes;  
forming in said interlayer insulating film a contact hole reaching one of said first impurity regions of said first transistor and said nitride film;  
introducing impurity into said semiconductor substrate through said contact hole to form a second impurity region overlapping with said one of said first impurity regions of said first